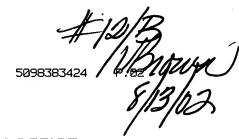
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WELLS ST JOHN PS



IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

plication Serial No	0
ing DateAugust 31, 200	0
ventorKeiji Jono et a	1.
signeeKMT Semiconductor, LTI	D
oup Art Unit281	1
aminer T.F. Tra	n
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le: Methods of Forming an Isolation Trench in a Semiconductor, Method	S
of Forming an Isolation Trench in a Surface of a Silicon Wafer, Method	ls
of Forming an Isolation Trench-Isolated Transistor, Trench-Isolate	d
Transistor, Trench Isolation Structures Formed in a Semiconductor	r,
Memory Cells and DRAM	

AMENDMENT DATED JULY 23, 2002 FAX RECEIVED

AUG 1 2 2002

To:

Assistant Commissioner for Patents

Washington, D.C. 20231

T.C. 2800

From:

Frederick M. Fliegel, Ph.D.

Tel. 509-624-4276; Fax 509-838-3424

Wells St. John P.S.

601 W. First Avenue, Suite 1300

Spokane, WA 99201-3828

Responsive to the Notice of Non-compliant Amendment dated July 23, 2002, Applicant comments as follows:

REMARKS

Applicants state on page 2 of the Response to October 12, 2001 Office Action, "Please amend the claims as follows:." However, the only amendments to the claims are cancellation of claims 33-61, no other